AMENDMENTS TO THE CLAIMS:

Please replace the claims with the claims provided in the listing below wherein status, amendments, additions and cancellations are indicated.

1. (Currently Amended) A transistor-type ferroelectric nonvolatile memory element having an MFMIS (metal-ferroelectric-metal-insulator-semiconductor) structure formed in a semiconductor substrate, comprising:

an MFM (metal-ferroelectric-metal) structure and an MIS (metal-insulator-semiconductor) structure vertically arranged with the MFM structure above a level of the MIS structure; and

means for increasing an effective area of a capacitance of the MIS structure as compared with the effective area of a capacitance of the MFM structure, the means for increasing the effective area including a ~~lower~~ substrate layer of the MIS structure being formed as one of a trench and a rugged portion such as to increase a surface area ~~thereof~~ of an interface of an insulator layer and [[a]] the substrate layer of the MIS structure.

2. (Currently Amended) A transistor-type ferroelectric nonvolatile memory element according to claim 1, wherein the trench is formed in the semiconductor substrate, the MIS structure is formed in the trench, the MFM structure is

laminated on the trench nearly in parallel with [[the]] a main surface of the semiconductor substrate, and means for increasing the effective area is the trench.

3. (Currently Amended) A transistor-type ferroelectric nonvolatile memory element according to claim 2, wherein the MIS structure is an MIS transistor of the nonvolatile memory element, [[the]] regions of source, base and drain of the MIS transistor are formed in the semiconductor substrate in order of source, base and drain from [[the]] a lower side of the semiconductor substrate, and the means for increasing the effective area is a gate structure of the MIS transistor formed in the semiconductor substrate on [[the]] an inner surface of the trench.

4. (Currently Amended) A transistor-type ferroelectric nonvolatile memory element according to claim 2, wherein the MIS structure is an MIS transistor of the nonvolatile memory element, [[the]] regions of source, base and drain of the MIS transistor are formed in the semiconductor substrate in order of drain, base and source from [[the]] a lower side of the semiconductor substrate, and the means for increasing the effective area is a gate structure of the MIS transistor formed in the semiconductor substrate on [[the]] an inner surface of the trench.

5. (Currently Amended) A transistor-type ferroelectric nonvolatile memory element according to claim 2, wherein the MIS structure is a MIS transistor of the nonvolatile memory element, and [[the]] regions of source and drain of the MIS transistor are separated by the trench.

6. (Previously Presented) A transistor-type ferroelectric nonvolatile memory element according to claim 1, wherein the MIS structure includes the rugged portion therein, the means for increasing the effective area is constituted by the rugged portion, the upper part of the MIS structure is flat, and the MFM structure is laminated thereon.

7. (Previously Presented) A transistor-type ferroelectric nonvolatile memory element according to claim 1, wherein the means for increasing the effective area is constituted by an MIM (metal-insulator-metal) structure provided between the MFM structure and the MIS structure.

8. (Original) A transistor-type ferroelectric nonvolatile memory element according to claims 2 to 7, wherein the effective area of a metal layer on the ferroelectric layer of the MFM structure is smaller than that of the ferroelectric layer.